ACCELERCOMM
SUPERCHARGED WIRELESS

5G NR LDPC Hardware Acceleration BBDEV Interface

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INTRODUCTION

AccelerComm's BBDEV interface enables our high performance 5G NR LDPC encoding and decoding IP solutions to be rapidly and efficiently used as hardware accelerators in industry standard servers using an open, standardized interface over a PCIe bus.

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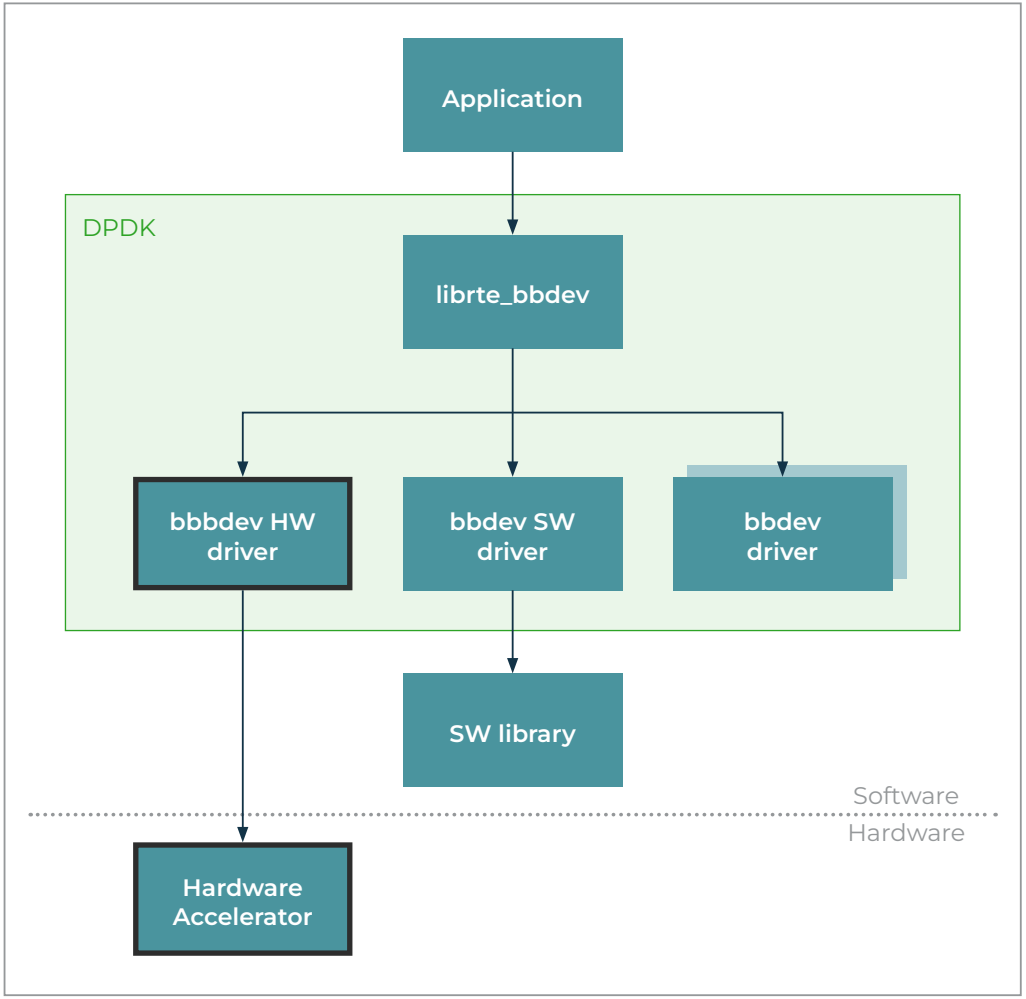
Low Density Parity Check (LDPC) channel coding or Forward Error Correction (FEC) is a key feature of 3GPP 5G New Radio (NR). The LDPC decoder is one of the most computationally intensive elements of a 5G modem, frequently representing up to 40% of the hardware resources needed to realise the Physical Layer (PHY). AccelerComm™ provides a range of high performance, flexible and efficient LDPC encoder and decoder IP specifically optimized for 5G NR.

With a move to software defined radios (SDR) a hardware accelerator is often used to offload the LDPC encoding and decoding from the CPUs performing the other PHY functions. This architecture is used in both the O-RAN Alliance reference architecture and Intel's FlexRAN platform.

The Data Plane Development Kit or DPDK is a widely adopted standard which includes the Wireless Baseband device library or BBDEV.

BBDEV provides a common programming framework that abstracts and decouples the application from the HW accelerator and its functions. At the time of publishing, BBDEV meets the requirements of both FlexRAN and O-RAN architectures.



BENEFITS

The AccelerComm™ BBDEV solution simplifies the creation of high performance 5G NR implementations on industry standard hardware using the DPDK.org toolkit:

- Performance optimized, production grade solution
- Standards based interface for rapid software development
- Fully compliant with Intel FlexRAN standards
- Fully compliant with O-RAN AAL Interface requirements
- Supports both AccelerComm™ LDPC chain in FPGA and AccelerComm™ LDPC wrapper with Xilinx SD-FEC provided in Ultrascale RF-SOC
- Lightweight interface simplifies integration
- Complex optimiaztion of PCIe interface transparent to application to maximize throughput
- Support for a range of industry standard PCIe 3.0 FPGA boards and FPGAs
- Available as a commercial solution with Xilinx PCIe cards
- Hardware reference kit available for customers implementing proprietary board design

PERFORMANCE

5G NR targets throughputs up to 20Gbps with sub 1ms latencies, across a wide range of radio conditions. A typical O-RAN Distributed Unit (DU) in a production environment will require a PCIe throughput in excess of 50Gbps which requires optimized software drivers to prevent the interface becoming a system throughput bottleneck.

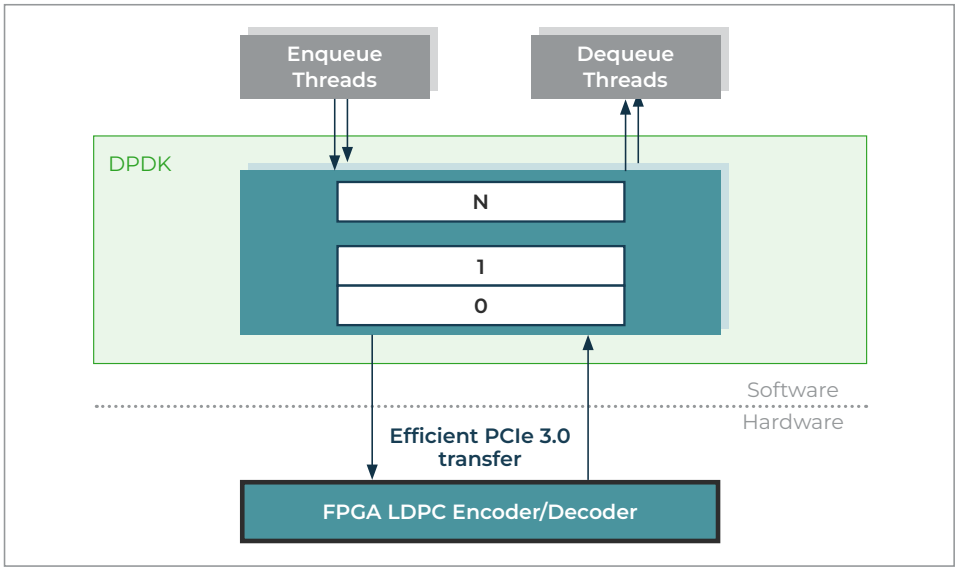
The AccelerComm™ BBDEV solution is engineered to overcome the limits of off-the-shelf drivers and can achieve speeds over 87% of the PCIe theoretical maximum. For example, in tests with a Xilinx T1 card (which uses a PCIe x8 Gen3 interface) and 2 CPU cores the decoder achieves a user throughput of 8 Gbps for decode or 20Gbps for encode.

AccelerComm™ is committed to vendor independence and is porting and optimizing the solution for a range of popular cards, contact our sales team for details.

BENEFITS

INTERFACE

The AccelerComm™ DPDK/BBDEV solution provides a simple interface between the application and the hardware accelerated encoder/decoder.



The application places a block of data for decoding or encoding in a standard memory buffer onto a queue and the processed data is returned onto the same or a separate queue.

The DPDK software and AccelerComm™ drivers handle queue management, the transfer of the data to the FPGA over the PCIe 3.0 bus, the processing and the return back over the PCIe 3.0 bus to the return queue.

For the decoding queue the software pre-processes the data to pack the LLRs and reduce PCIe bandwidth. The AccelerComm™ IP on the card unpacks the LLRs with no loss of decoder performance.

REFERENCE KIT

In order to further accelerate the development cycle, AccelerComm™ provide a hardware reference kit, a PCIe board with pre-programmed FPGA if required, together with the BBDEV test bench which enables developers to simulate and test the APIs to verify operation before testing with the application.

DESIGN SUPPORT

As well as providing support for the BBDEV interface AccelerComm™ provide industry leading support for the core LDPC IP product suite including a full test bench to prove 3GPP conformance that can be used in the most popular simulation tools, Mentor ModelSim® or Questa® and Cadence Xcelium®, and a bit accurate C model is also included for use in user simulations or in MATLAB.

AccelerComm™ provides support services to customers to help them with the integration of the IP into their designs, but typically this is a very straightforward process.

Our flexible IP can be configured to closely match the requirements of a wide range of designs, and then the combination of simple interfaces, complete documentation and supporting test harnesses and reference kits, backed up by our experienced support team mean that IP can be integrated and running within a day.

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AccelerComm™ is a semiconductor IP-core company that provides patented physical layer solutions. Our team has a proven track-record of signal processing and IP expertise, from developing and optimizing algorithms through to their implementation and delivery in FPGA and ASIC architectures. With more than 100 published IEEE papers and numerous citations for our work in 3GPP RAN1, we are having a significant impact on the mobile communications world.

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